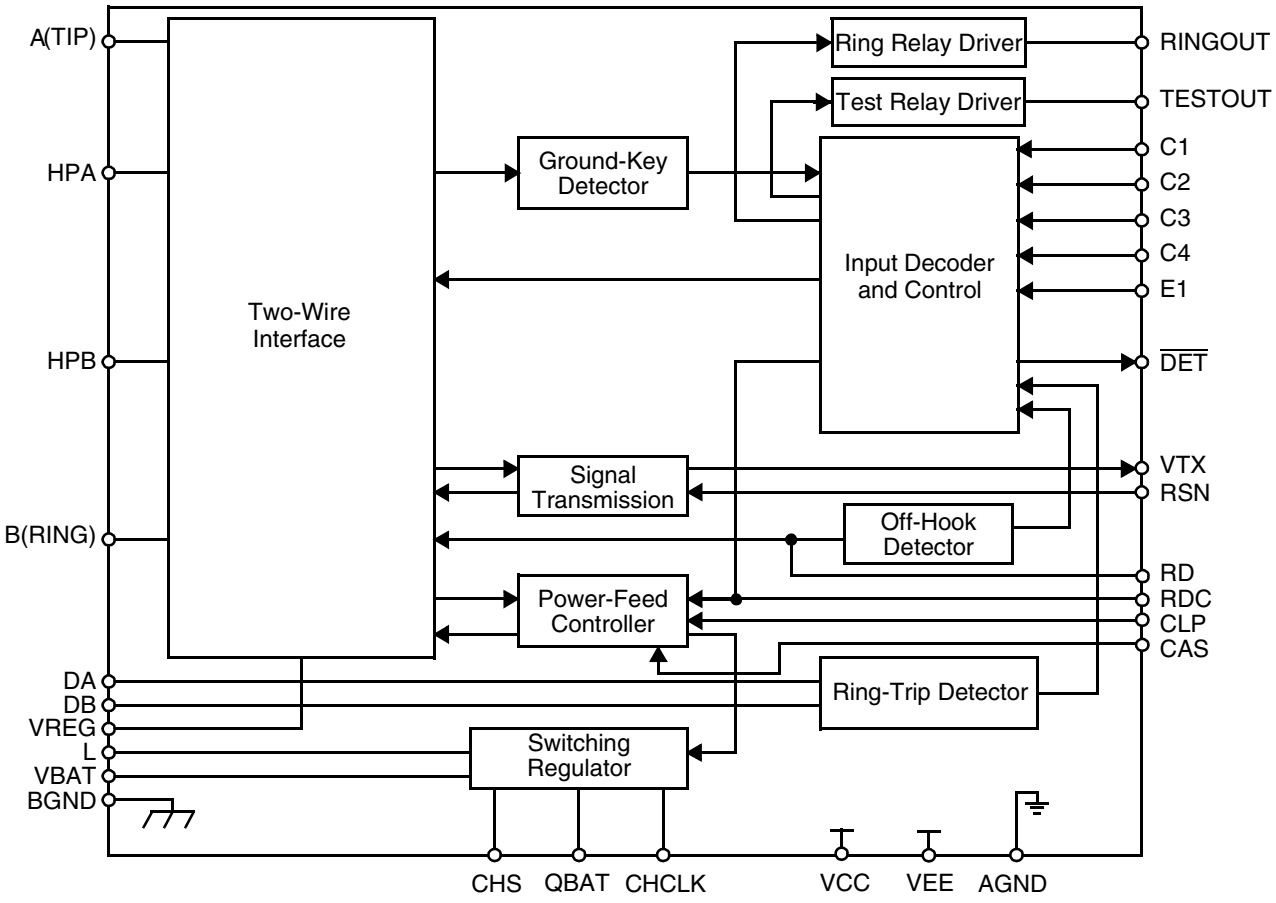
Am79578

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Programmable constant-resistance feed**
- **Programmable loop-detect threshold**
- **On-chip switching regulator for low-power dissipation**
- **Programmable Current Limit (CLP)**
- **Ground-key detector**
- **Two-wire impedance set by single external impedance**
- **Polarity reversal feature**
- **Tip Open state for ground-start lines**
- **Test relay driver**
- **On-hook transmission**
- **High Open Circuit state (HOC)**

BLOCK DIAGRAM



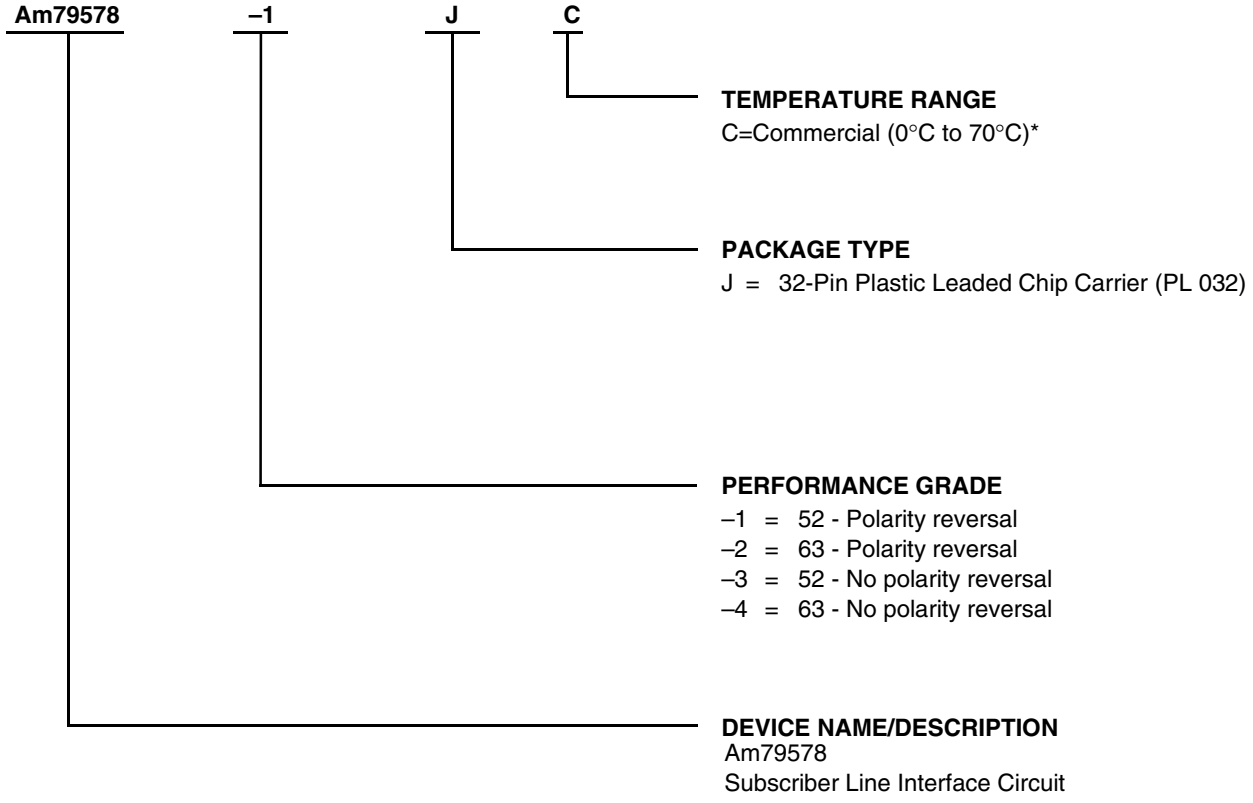
21777A-001

Publication# **080212** Rev: **C** Amendment: **/0**
Issue Date: **October 1999**

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79578	–1 –2 –3 –4	JC

Valid Combinations

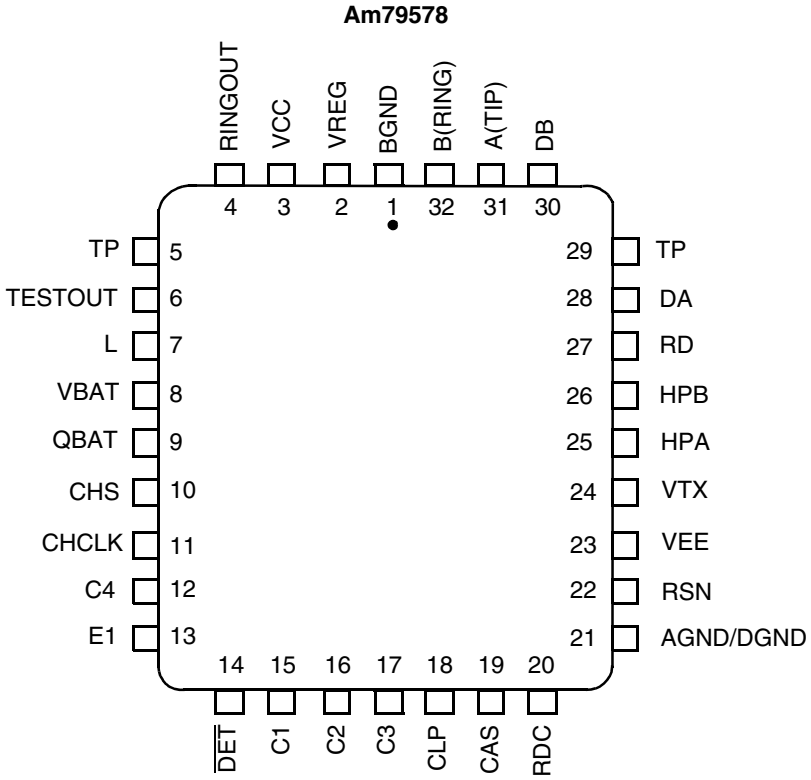
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's products.

Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAM

Top View



21777A-002

Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate (QBAT).*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
C4	Input	TTL compatible. A logic Low enables the driver.
CAS	Capacitor	Anti-saturation capacitor. Filters reference voltage when operating in anti-saturation region.
CHCLK	Input	Input to switching regulator (TTL compatible). Frequency = 256 kHz (Nominal).
CHS	Input	Chopper Stabilization. Connection for external stabilization components.
CLP	—	Current limit programming. Open = 30 mA current limit, short to VEE = 50 mA current limit, a resistor to VEE = 30–50 mA current limit, with a programmed feed of 400 Ω, including two 20 Ω fuse resistors.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Detector. When enabled, logic Low indicates that the selected detector is tripped Logic inputs C3–C1 and E1 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	E1 = High connects the ground-key detector to $\overline{\text{DET}}$, and E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$.
HPA	Capacitor	High-pass filter capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor. B(RING) side of high-pass filter capacitor.
L	Output	Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V pulse waveform; isolated from sensitive circuits. You must keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Quiet battery. Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Threshold modification and filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the Receiver Summing Node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver. Open collector Darlington pull down to BGND.
RSN	Input	Receiving Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) = 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Route the 256 kHz chopper clock and switch lines away from the RSN node.
TESTOUT	Output	Test relay driver. Open collector Darlington pull down.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.
VBAT	Battery	Battery supply. Connected through an external protection diode.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VREG	Input	Regulated voltage. Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . .–0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND . . .+0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND . . +0.4 V to –70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.*

BGND with respect to
AGND/DGND . . . . . .+1.0 V to –3.0 V

A(TIP) or B(RING) to BGND:

Continuous . . . . . –70 V to +1.0 V
10 ms (f = 0.1 Hz) . . . . . –70 V to +5.0 V
1 µs (f = 0.1 Hz) . . . . . .–90 V to +10 V
250 ns (f = 0.1 Hz) . . . . . .–120 V to +15 V

Current from A(TIP) or B(RING). . . . . .±150 mA

Voltage on RINGOUT. . . . BGND to 70 V above Q_{BAT}

Voltage on TESTOUT. . . . BGND to 70 V above Q_{BAT}

Current through relay drivers . . . . . 60 mA

Voltage on ring-trip inputs
(DA and DB) . . . . . VBAT to 0 V

Current into ring-trip inputs . . . . . .±10 mA

Peak current into regulator switch (L pin). . . . 150 mA

Switcher transient peak off
voltage on L pin. . . . . +1.0 V

C4–C1, E1, CHCLK to
AGND/DGND . . . . . .–0.4 V to VCC + 0.4 V

Maximum power dissipation, (see note). . . . T_A = 70°C

In 32-pin PLCC package. . . . . 1.74 W

Note: *Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{EE} . . . . . –4.75 V to –5.25 V

V_{BAT} . . . . . –40 V to –58 V

AGND/DGND . . . . . 0 V

BGND with respect to
AGND/DGND. . . . . –100 mV to +100 mV

Load Resistance on VTX to ground . . . . . 10 kΩ min

Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog (V_{TX}) output impedance			3		Ω	
Analog (V_{TX}) output offset	0°C to +70°C –40°C to +85°C	–40 –50		+40 +50	mV	— 4
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	Ω	4
Longitudinal impedance at A or B	0 Hz to 100 Hz			35		
Overload level, Z_{2WIN} = 600 Ω	4-wire 2-wire	–3.1		+3.1	Vpk	2
Transmission Performance						
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz 500 Hz to 2.5 kHz 2500 Hz to 3.4 kHz	26 26 20			dB	4, 10
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz –1, –3* Normal polarity 0°C to 70°C –2, –4 Normal polarity –40°C to +85°C –2, –4 Reverse polarity –2, –4		52 63 58 54		dB	— — 4 —
	1 kHz to 3.4 kHz –1, –3* Normal polarity 0°C to 70°C –2, –4 Normal polarity –40°C to +85°C –2, –4 Reverse polarity –2, –4		52 58 54 54			— — 4 —
Longitudinal signal generation 4-L	300 Hz to 800 Hz	42				
Longitudinal current capability per wire	Active state HOC state		25 18		mArms	4
Insertion Loss and Balance Return Signal (2- to 4-Wire, 4- to 2-Wire, and 4- to 4-Wire, See Test Circuits A and B)						
Gain accuracy over temperature	0 dBm, 1 kHz 0°C to 70°C –40°C to +85°C	–0.15 –0.20	0 0	+0.15 +0.20	dB	— 4
Gain accuracy over frequency	300 Hz to 3.4 kHz 0°C to 70°C relative to 1 kHz –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		— 4
Gain tracking	+3 dBm to –55 dBm 0°C to 70°C relative to 0 dBm –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		— 4
Gain accuracy, on hook		–0.50		+0.50		4
Group delay	0 dBm, 1 kHz		5.3		µs	4, 12
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire, See Test Circuits A and B)						
Total harmonic distortion	0 dBm, 300 Hz to 3.4 kHz +9 dBm, 300 Hz to 3.4 kHz		–64 –55	–50 –40	dB	
Harmonic distortion, long loop	V_{BAT} = –50 V, R_L = 1900 Ω, Vpk = 2.5 V			–40		
Harmonic distortion, on hook	V_{BAT} = –50 V, Vpk = 500 mV			–36		
Idle Channel Noise						
Psophometric weighted noise	2-wire 4-wire		–83	–78	dBmp	

Note:
** Performance Grade*

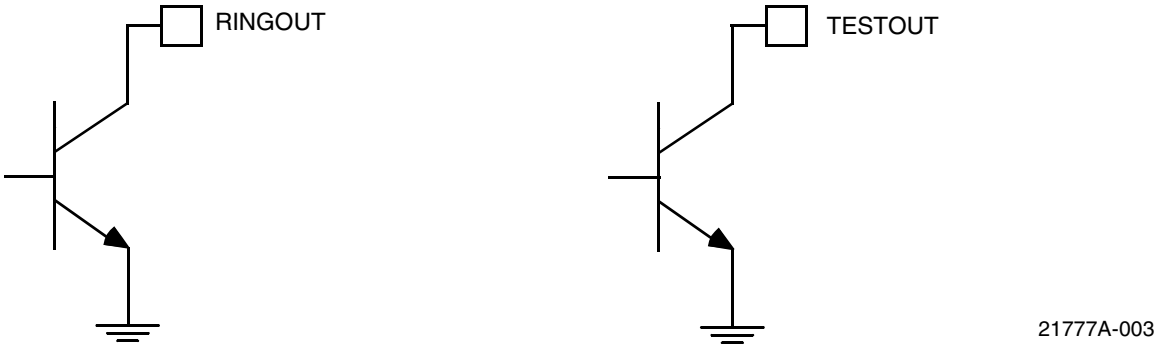
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Single Frequency Out-of-Band Noise (See Test Circuit E)						
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics		–76 –76 –57		dBm	4, 5, 9 4, 5, 9 4, 5
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics		–70 –85 –57		dBm	4, 5, 9 4, 5, 9 4, 5
Line Characteristics (See Figure 1) R_{FEED} = 400 Ω						
Apparent battery voltage	Active		50		V	
I_L, Long loops, Active state	V_{BAT} = –50 V, R_L = 1900 Ω	19			mA	
I_L, Tip Open state				1.0	mA	
I_L, Open Circuit state	R_L = 0 Ω			1.0	mA	
Open Circuit voltage, Active state	V_{BAT} = –50 V, T_A = 25°C	41.5	43		V	
Open Circuit voltage, HOC state	V_{BAT} = –50 V		V_{BAT} – 2		V	7
Fault current limit, I_LLIM (I_{AX} + I_{BX})	A and B shorted to GND			130	mA	
Active current limit	R_{CLP} = open, R_L = 210 Ω R_{CLP} = short to V_{EE}, R_L = 210 Ω R_{CLP} = 170 to V_{EE}, R_L = 210 Ω	25 45 35	30 50 40	35 55 45	mA	
Power Dissipation, Normal Polarity						
On hook, Open Circuit state			35	80	mW	
On hook, HOC state			135	250	mW	
On hook, Active state			200	300	mW	
Off hook, HOC state			500	750	mW	
Off hook, Active state			650	1000	mW	
Supply Currents						
V_{CC} on-hook supply current	Open Circuit HOC Active		3.0 6.0 8.0	4.5 10.0 13.0	mA	
V_{EE} on-hook supply current	Open Circuit HOC Active		1.0 2.3 3.0	2.3 3.7 6.0	mA	
V_{BAT} on-hook supply current	Open Circuit HOC Active		0.4 3.2 4.5	1.0 5.5 7.0	mA	

ELECTRICAL CHARACTERISTICS (continued)

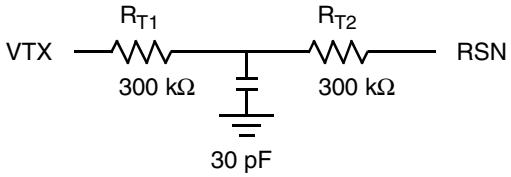
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Power Supply Rejection Ratio (V_{RIPPLE} = 50 mVrms)						
V_{CC}	50 Hz to 3.4 kHz	30	45		dB	6
	3.4 kHz to 50 kHz	25	40			
V_{EE}	50 Hz to 3.4 kHz	25	40			
	3.4 kHz to 50 kHz	10	25			
V_{BAT}	50 Hz to 3.4 kHz	30	45			
	3.4 kHz to 50 kHz	25	40			
Off-Hook Detector						
Current threshold accuracy	I_{DET} = 365/R_D Nominal	–20		+20	%	
Current threshold, Tip Open state	I_{DET} = 712/R_D	–20		+20		
Ground-Key Detector Thresholds, Active State, (See Test Circuit F)						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	kΩ	
Ground-key current threshold	B(RING) to GND		9		mA	8
	Midpoint to GND		9			
Ring-Trip Detector Input						
Bias current		–5	–0.05		µA	
Offset voltage	Source resistance 0 Ω to 2 MΩ	–50	0	+50	mV	11
Logic Inputs (C4–C1, E1, and CHCLK)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current, except E1		–75		40	µA	
Input High current, E1		–75		45		
Input Low current		–0.4			mA	
Logic Output ($\overline{DET}$)						
Output Low voltage	I_{OUT} = 0.8 mA			0.4	V	
Output High voltage	I_{OUT} = –0.1 mA	2.4				
Relay Driver Outputs (RINGOUT, TESTOUT)						
On voltage	25 mA sink		1.0	1.5	V	
Off leakage			0.5	100	µA	

RELAY DRIVER SCHEMATICS



Notes:

1. *Unless otherwise noted, test conditions are BAT = –52 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 0.22 µF, $R_{DC1} = R_{DC2}$ = 9 kΩ, C_{DC} = 0.2 µF, R_D = 51.1 kΩ, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 600 kΩ resistive, receive input summing impedance (Z_{RX}) = 300 kΩ resistive. (See Table 2 for component formulas.) Series battery resistor = 22 Ω.*
2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *These tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω for frequencies below 12 kHz and 135 Ω for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
7. *The open circuit voltage will limit to 50 V typical at high battery voltages ($|V_{BAT}| > 52$ V).*
8. *"Midpoint" is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).*
9. *Fundamental and harmonics from 256 kHz switch-regulator chopper are not included.*
10. *Assumes the following Z_T network:*



11. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design purposes only.*
12. *Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network reduces the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated by using the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Decoding

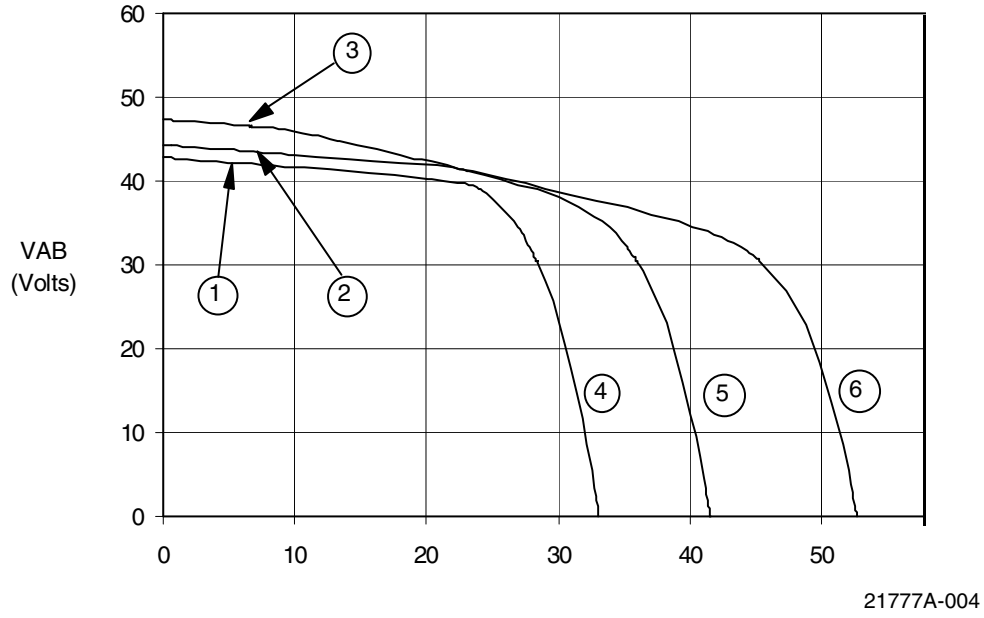
				$\overline{DET}$ Output	
State	**C3**	**C2**	**C1**	**Two-Wire Status**	**E1 = 0**	**E1 = 1**
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	High Open Circuit (HOC)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	—
5	1	0	1	Reserved	—	—
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	HOC Polarity Reversal	Loop detector	Ground key

Note:
The HOC state offers higher open circuit voltage than the Active state by disabling the anti-saturation circuitry. Idle power dissipation in the HOC state is less than that in the Active state. On-hook transmission is not supported in the HOC state below a $|V_{BAT}|$ of 56 V.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{1000 \bullet Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin, Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = 50 \ (R_{FEED} - 2R_F)$ $C_{DC} = 1.5 \text{ ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = \frac{365}{I_T}, \ C_D = \frac{0.5 \text{ ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.

DC FEED CHARACTERISTICS

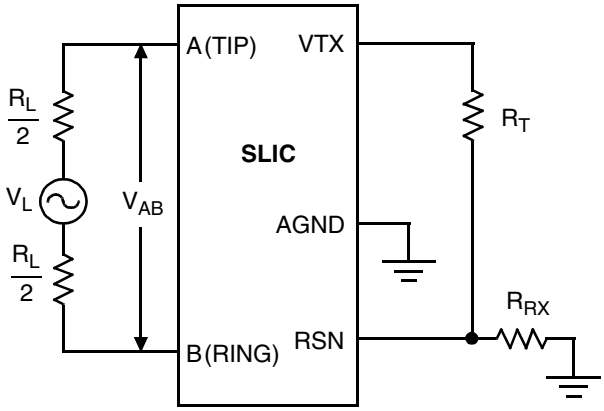


Notes:

1. V_{BAT} = –50 V
2. V_{BAT} = –52 V
3. V_{BAT} = –56 V
4. R_{CLP} = Open
5. R_{CLP} = 170 kΩ
6. $R_{CLP} = V_{EE}$

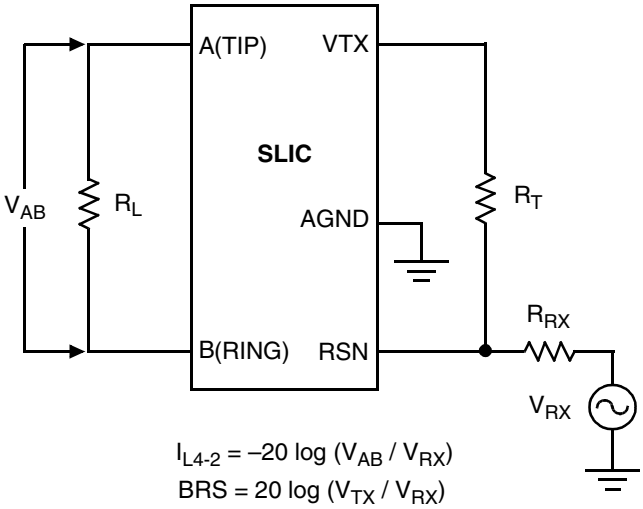
Figure 1. DC Feed Characteristics

TEST CIRCUITS



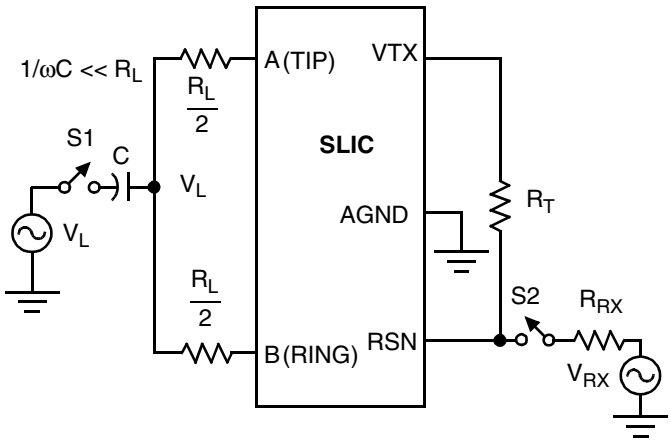
$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$

A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$
$BRS = 20 \log (V_{TX} / V_{RX})$

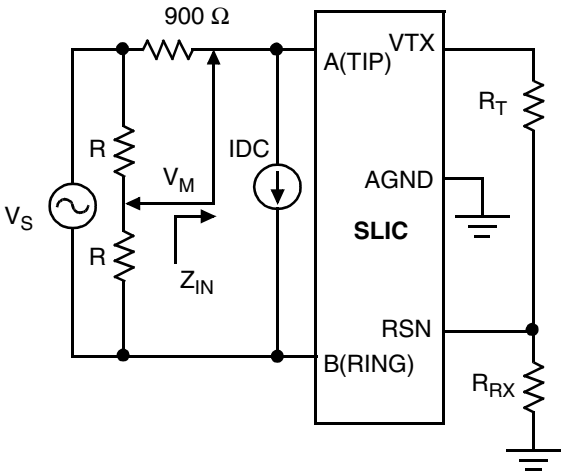
B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = $-20 \log (V_{AB} / V_L)$
L-4 Long. Bal. = $-20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

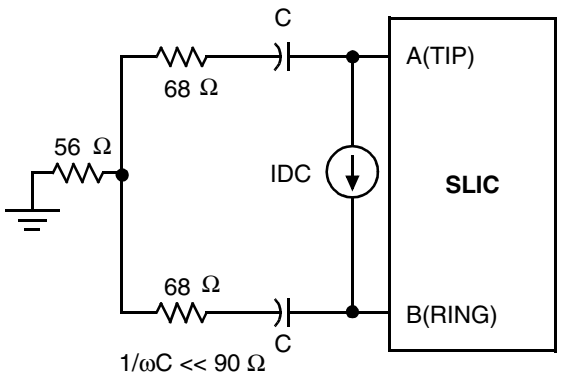


Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).

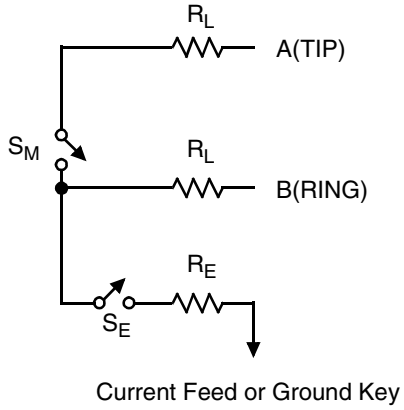
$R_L = -20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

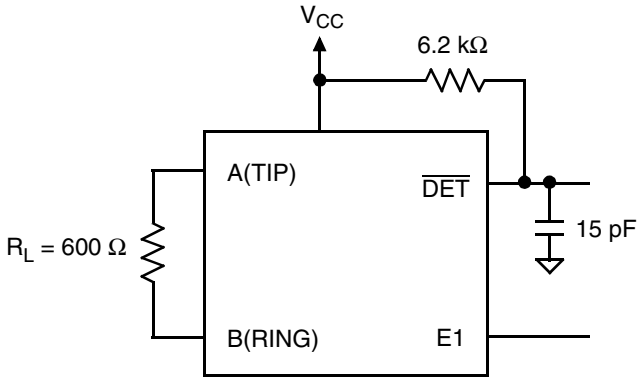
TEST CIRCUITS (continued)



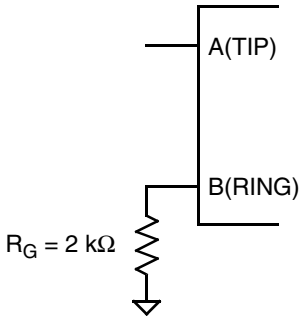
E. Single-Frequency Noise



F. Ground-Key Detection

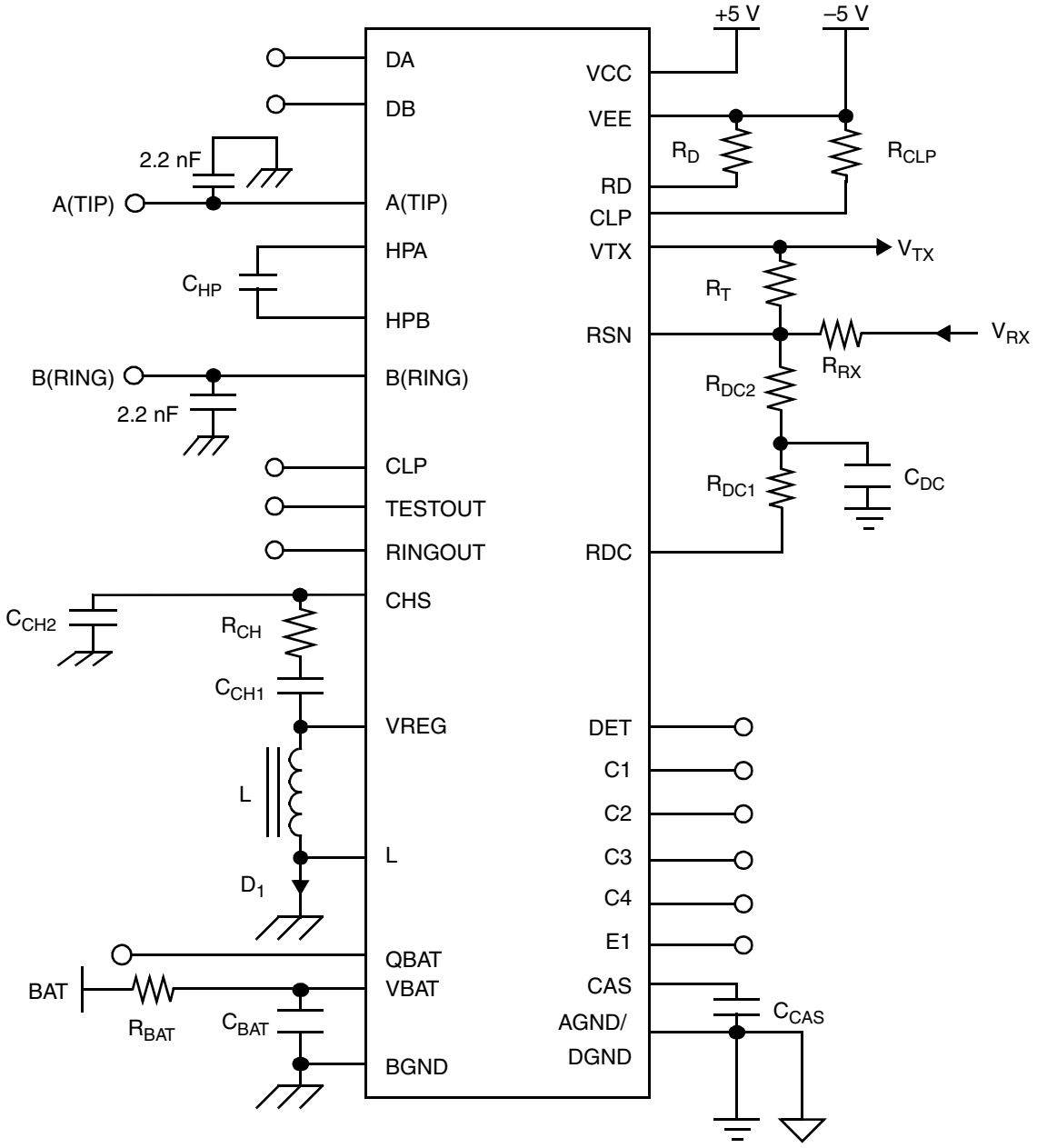


G. Loop-Detector Switching



H. Ground-Key Switching

TEST CIRCUITS (continued)



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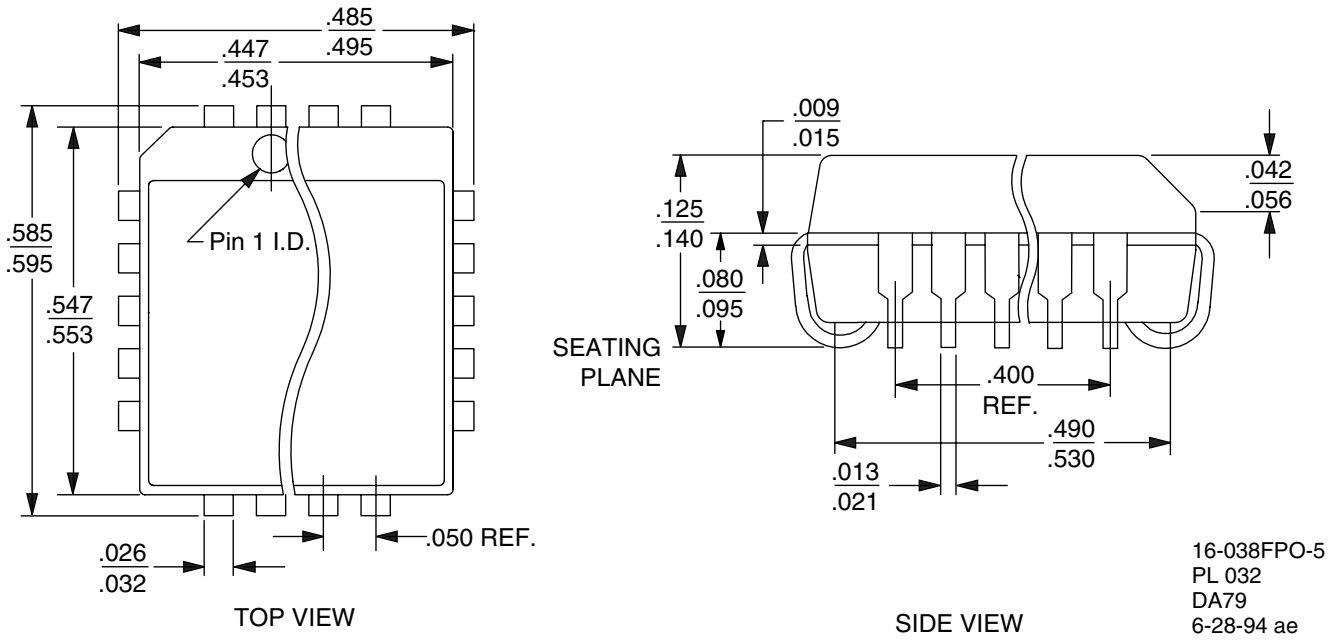
I. Am79578 Test Circuit

PHYSICAL DIMENSIONS

PL032



REVISION SUMMARY

Revision A to Revision B

- Minor changes to the data sheet style and format were made to conform to Legerity standards.
- In the Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”

Revision B to Revision C

- The physical dimensions (PL032) were added to the Physical Dimensions section.
- Deleted the Ceramic DIP and Plastic DIP packages and references to them.
- Updated the Pin Description table to correct inconsistencies.

Notes:

Notes:

Legerity provides silicon solutions that enhance the performance, speeds time-to-market, and lowers the system cost of our customers' products. By combining process, design, systems architecture, and a complete set of software and hardware support tools with unparalleled factory and worldwide field applications support, Legerity ensures its customers enjoy a smoother design experience. It is this commitment to our customers that places Legerity in a class by itself.

P.O. Box 18200
Austin, Texas 78760-8200

Telephone: (512) 228-5400
Fax: (512) 228-5510
North America Toll Free: (800) 432-4009

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